IOSR Journal of Electronics and Communication Engineering (IOSR-JECE)
e-ISSN: 2278-2834,p- ISSN: 2278-8735.Volume 9, Issue 3, Ver. IV (May - Jun. 2014), PP 38-43
www.iosrjournals.org

Fault Injection Based Channel Allocation Of Noc Architecture For Ldpc Decoders

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Abstract: *Network-on-chip (NoC) architectures are emerging for the highly scalable, reliable, and modular on-chip communication infrastructure platform. The NoC architecture uses layered protocols and packet-switched networks which consist of on-chip routers, links, and network interfaces on a predefined topology. In this Project ,we design network-on-chip which is based on the Cartesian network environment.*

This project proposes the new Cartesian topology which is uded to reduce network routing time, and it is an suitable alternate to network design and implementation.

The cartesian Network-On-Chip can be modelled using Verilog HDL and simulated using Modelsim software&Quartus II.

Keywords: *Network-on-Chip (NoC), Routing, Switching, Cut-through,Cartesian*

I. Introduction

Cartesian routing is a fast packet routing mechanism intended for geographic addresses and can effectively accelerate the packet routing process within a local or metropolitan environment. The wide area Cartesian routing described in this paper is an extension of the Cartesian routing algorithms designed to make the exchange of internet work packets between geographical regions possible. It also introduces a new hierarchical structure for the entire Internet. The proposed Internet is viewed as a hierarchy of networks consisting of routers. At the highest level of this hierarchy, major routers exchange packets between large geopolitical areas such as countries, states, or provinces. At the lowest level of the structure, packets are routed between local routers in small geographical regions ranging from an office to a small town. There are only four layers in this structure and at each layer Cartesian routing is employed to send packets from the source router to the destination.

The wide-area Cartesian Routing algorithm overcomes these problems by creating a hierarchical network consisting of two or more layers. Each network at a given layer encompasses one or more networks. Each network, regardless of its layer, employees the Cartesian Routing algorithm for packet routing. Two extensions to the original Cartesian Routing algorithm are required: each network (except for the highest) requires an internet work router that can direct packets destined for other networks “up” to the encompassing network.

The address structure reflects the network structure, with specific fields in the address associated with each layer.

II. Cartesian Networks

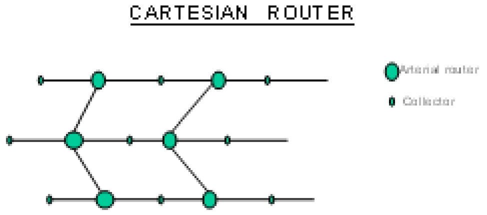


Fig 1. Cartesian router

A Cartesian network consists of a set of *collectors* and one or more *arterials.*Each collector is a chain of *collector routers* running east-west and sharing a common latitude. Collector routers have two side ports (east and west) to exchange packets’ horizontally’. Each collector router also has a *bottom* Port which allows it to connect to a set of local hosts. Arterials exchange packets between collectors. Each arterial router, except the most northerly and the most southerly has, at least, four ports (north, south, east and west). Arterials need not share a common longitude. In a Cartesian network, the imposed topological structure relieves each router from maintaining routing tables. Each router is bound to a unique pair of addresses, the state information is minimal, and each router maintains the accessibility of arterials to its west and east.

In Cartesian routing, each arterial issues *Arterial This Way* (ATW) control packets during its initialization process. An ATW tells the receiving collector router if an arterial is accessible through the incoming port. An ATW also specifies what kind of connection is accessible via the incoming port: north, south, north and south or neither. Upon receiving an ATW, each collector router updates its *Arterial Direction Indicator* (ADI) and forwards the ATW to the opposite port. ATWs are also used to establish

Virtual Arterials , constructed in situations where it is physically impossible for an arterial to span two collectors. The ADI points in the direction of the arterial router (i.e., east or west) and indicates whether the arterial router has a connection to the north, the south, or both. Figure 1 illustrates a Cartesian network.

2.2 Cartesian Routing

Packets can arrive on either a west or east port of a collector router. Packets intended for a different latitude are forwarded out the opposite port from which they are received. The ADI determines the packet’s initial direction on the collector router when a packet arrives on the bottom port of a collector router. In deciding a packet’s initial direction, the router first compares the packet’s destination address with its own address. The packet will be forwarded in the direction of the destination if the destination latitude is the same as the collectors. The packet is forwarded in the direction of the ADI if the destination is on different latitude.

2.3 Wide Areas Cartesian Networks

A Cartesian network provides a straightforward topological structure that relieves collector routers from the need to maintain routing tables. However, it would be unrealistic to implement a single worldwide Cartesian network. Such a widespread Cartesian network, for example, requires every packet destined for a router with the same latitude identifier as the source router’s latitude identifier to visit all the collector routers. It is also necessary for such a network to have one collector for every possible latitude. These limitations suggest that implementing a single worldwide Cartesian network would be impractical. An alternative to a worldwide Cartesian network is to create a set of smaller Cartesian networks and implement a mechanism for interchanging packets between them. One approach to interchanging packets between Cartesian networks is to forward packets towards their destinations.

ADDRESS	FUNCTIONS

Dest_lat=node_lat
Dest_long=node_long
	Router keeps the Packet

Dest_lat>node_lat Dest_long>node_long	Packet routed to North Port
Dest_lat<node_lat Dest_long>node_long	Packet routed to South Port
Dest_lat=node_lat Dest_long>node_long	Packet routed to East Port
Dest_long<node_long	Packet Discarded

Table 1:4-port Routing algorithm

When a packet reaches the boundary of a network it “falls off ” the edge and is delivered to a special router to be forwarded towards the destination address. The process of routing a packet from one network to another using this approach becomes problematic when networks are *interleaved* or *overlapped* .Two networks are considered interleaved if there is at least one collector router on one of the networks where its longitude identifier lies between the longitude identifiers of two collectors from the other network and its latitude identifier lies between the latitude identifiers of two collectors from the other network. Figure illustrates two interleaved networks. Two networks are said to be overlapped if there is at least one collector router on one of the networks where its longitude identifier lies between the longitude identifiers of two collectors from the other network and all three of them share the same latitude identifier. Figure illustrates two overlapped networks.

An alternative method for delivering a packet to its destination is to find the destination network address and then to route the packet to the destination network by using Cartesian routing algorithms. This implies that each network must be identifiable using the packet’s destination address. If we assume that each network has a rectangular shape, recognizing the destination network is a matter of comparing the packet’s destination address with the network’s boundaries. However, there are a number of reasons to assume that it would be unrealistic to expect networks to have rectangular borders: geographical barriers and political jurisdictions, for example. Since Cartesian routing uses latitude and longitude pairs to identify the source and the destination addresses of packets, this information is not sufficient to determine to which network a collector/arterial belongs in the case of interleaved and overlapped networks. This, in turn, suggests that an additional set of information is required to identify to which network a collector or arterial is connected. To achieve this, the authors propose a hierarchical structure for Cartesian networks. In the next section the possibility of multiple-layer Cartesian networks as a solution for interchanging packets between arbitrary shaped interleaved and overlapped Cartesian networks are explained. In the remainder of this paper, the terms "wide area Cartesian networks" and "multiple-layer Cartesian networks" are used interchangeably.

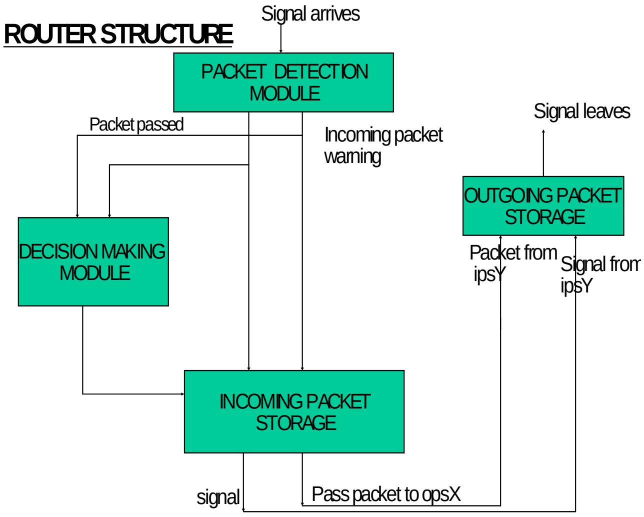


Fig 2: Router Structure

III. Multiple-Layer Cartesian Networks

Multiple-layer Cartesian networks impose a new set of topological dependencies among a set of Cartesian networks, such that interchanging packets between networks is feasible without creating and maintaining routing tables. Generally, in multiple layer Cartesian networks, the idea of Cartesian networks is expanded in a larger scale using a hierarchical structure

3.1 Decision Making Module

Multiple-layer Cartesian networks have a hierarchical structure. The highest layer of the hierarchy is a single Cartesian network. Each underlying layer consists of a set of mutually disjoint Cartesian networks (i.e., they are physically disjoint and share no collector or arterial router); however, networks in the same layer can be interleaved or overlapped.

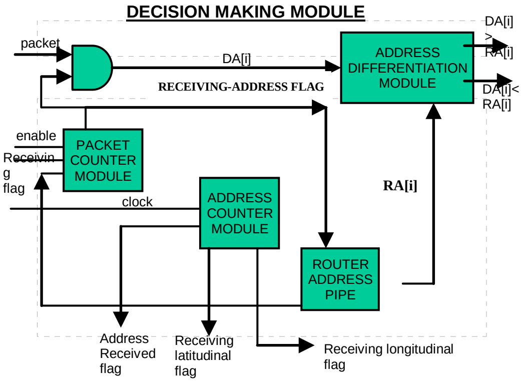


Fig 3: Decision Making Module

The PCM(Packet Counter Module) strips the destination address from the packet. It counts the incoming packet bits and sets the RECEIVING-ADDRESS flag when the first bit of the address is read .The ACM(Address Counter Module) keeps the track of the number of address bits that have been read. It indicates which portion of the address is being received(latitude or longitude) and if the entire address is received, it sets the ADDRESS-RECEIVED flag. When the ADDRESS-RECEIVED flag is set, the IPS is told to keep the packet. The RAP stores the router address and pipes it our serially so that it can be compared with the incoming destination address.

The Router address is static value and is kept in non-volatile memory for long term storage. The ADM simply compares the i-th bit of the destination address to the i-th bit of the router address as the destination address is read in to the DMM.If the DA does not equal to RA, the ADM tells the incoming packet storage(IPS) module to destroy the stored packet

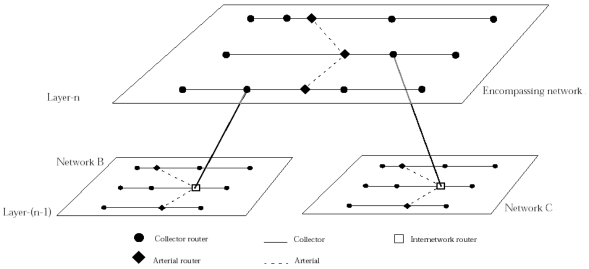


Figure 4: An encompassing network (A) and two encompassed networks (B and C).

3.2 Router Identification

In a Cartesian network, each router is bound to a Cartesian address . Whereas, in a multiple-layer Cartesian network, each router is bound to an *identifier* . The identifier of a router at layer-m of an m-layer Cartesian network is the same as its Cartesian address. An identifier of a router at lower layers is the identifier of its immediate encompassing router, followed by the Cartesian address of the router itself, meaning that an identifiers an ordered list of Cartesian addresses. For example, routers at layer-(m-1) maintain the Cartesian address of the router that represents the network to which they belong, followed by their own Cartesian address. In general, in an m-layer Cartesian network, each router at layer-n maintains a list of (m-n+1) ordered Cartesian addresses, where . For example, routers at the lowest layer of the hierarchy, layer-1, which are connected to local hosts through their bottom ports, are bound to m ordered Cartesian addresses: m-1 correspond to the identifier of the encompassing router at layer-2, and one, the Cartesian address of the router itself. Figure 5 illustrates the hierarchical addressing structure of an identifier for a router at layer-n of an m-layer Cartesian network. The hierarchical addressing structure overcomes the problems with both interleaved and overlapped networks since every router in the hierarchy has a unique address. It also enables a router in a network at layer to determine if a packet is local to the network or not. A packet is said to be *local* to a network if the network encompasses the destination address of the packet. A router can determine this by comparing the most significant m-n Cartesian addresses of the packet’s destination address with the first m-n Cartesian addresses of its own identifier. In an m-layer Cartesian network, each collector router at layer-n is bound to an identifier which is a list of m-n+1 Cartesian addresses. A packet can enter a network at layer-n through the bottom port of a collector router or the top port of the network’s IR. Packets received on the bottom port of a collector router are either local or non-local to the network, as described above.

PACKET FORMAT

SOP→Start of Packet(6 bits---6’b111111)
EOP→End of Packet(6 bits---6’b111111)
M →Cast(Unicast-4’b0000,Multicast-’b0001)
DLAT→Destination Latitude
DLON→Destination Longitude

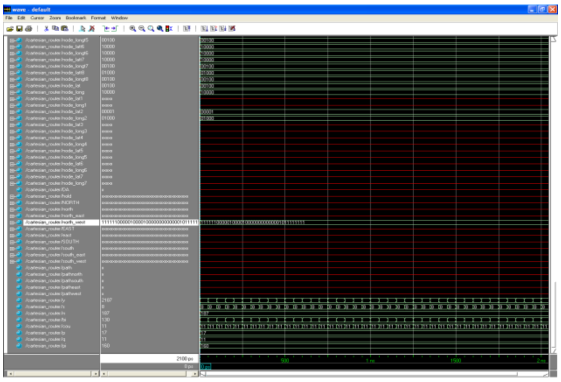
SOP	M	DLAT	DLON	SLAT	SLONG	DATA	EOP

3.3*Packet Routing*

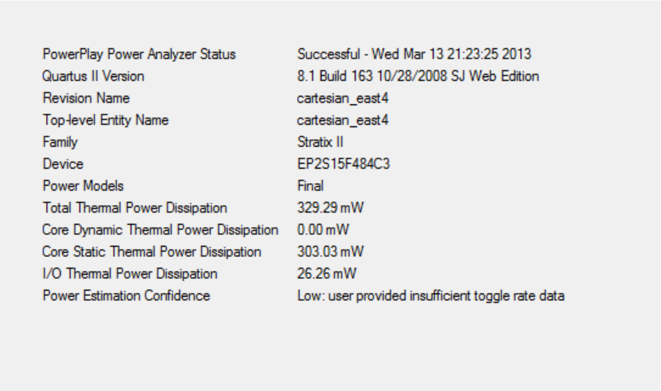
When a packet is found to be local, that is, the network encompasses the destination address, the router “tags” the packet as a local packet by setting a single bit of the packet’s address called the *local bit* . When a packet is local to a network at layer-n, the (m-n+1) th Cartesian address of the packet's destination address is used to route the packet in the network using Cartesian routing algorithm. For example, at layer-m, the first Cartesian address is used for Cartesian routing, while at layer-1 the mth address is used. When a packet is received by a router on its bottom port, the address is Cartesian address of the encompassing router at layer-(m-1) inspected. Non-local packets must be sent towards the network's IR in order to be delivered to the encompassing network. The router clears the local bit and forwards the packet towards the IR. Forwarding a packet to the IR requires that each collector router and arterial maintains an *Internetwork Router Direction Indicator* or IRDI. The IRDI determines if the internetwork router is accessible through the west port, east port or neither, in the case of collector routers; or whether it is accessible through the north port, south port or neither, in the case of arterials. If the packet is determined to be non-local, it is forwarded in the direction specified by the IRDI. When the IRDI indicates that IR is not accessible, the packet is dropped and a message is returned to the source notifying that the destination address is not reachable.

A collector router that receives a packet on its west or east port checks the local bit; if set the Cartesian routing algorithm is employed to route the packet, otherwise the packet is forwarded to the opposite port. When a packet enters a network through the top port of the network's IR, the packet is guaranteed to be local, since this has already been verified by the encompassing network. Upon receiving the packet, the IR sets the local bit and then applies the Cartesian routing algorithm on the (m-n+1) th Cartesian address of the packet's destination address.

IV. Simulation Results



4.1.Router Design simulation Result



PowerPlay Power Analyzer Status	Successful - Wed Mar 13 21:23:25 2013
Quartus II Version	8.1 Build 163 10/28/2008 SJ Web Edition
Revision Name	cartesian_east4
Top-level Entity Name	cartesian_east4
Family	Stratix II
Device	EP2S15F484C3
Power Models	Final
Total Thermal Power Dissipation	329.29 mW
Core Dynamic Thermal Power Dissipation	0.00 mW
Core Static Thermal Power Dissipation	303.03 mW
I/O Thermal Power Dissipation	26.26 mW
Power Estimation Confidence	Low: user provided insufficient toggle rate data

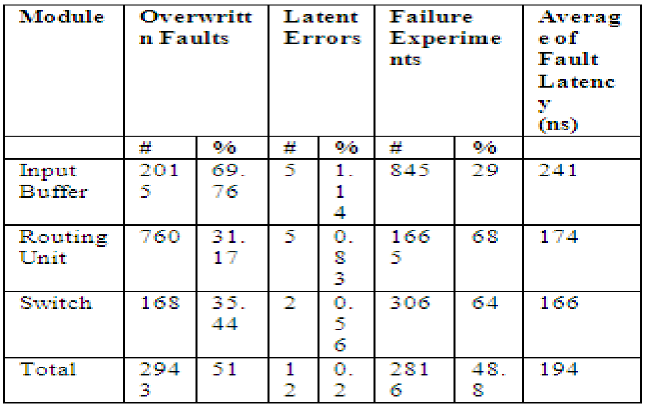
4.2 Power Analysis of Port

V. Conclusion

In Previous work, they designed conventional router which uses a routing table to determine whether to keep, forward or discard the packets. As networks grow in size, the memory requirements of the routing tables increases proportionally. The average search time increases as the routing table increases. ASIC based router design.

In our Proposed work, the New cartesian network is designed, which is Independent of routing table.It is the High speed network transmission when compared with existing work.

4.3 Throughput Analysis



Module	Overwritten Faults		Latent Errors		Failure Experiments		Average of Fault Latency (ns)
	#	%	#	%	#	%	
Input Buffer	2015	69.76	5	1.14	845	29	241
Routing Unit	760	31.17	5	0.83	1665	68	174
Switch	168	35.44	2	0.56	306	64	166
Total	2943	51	12	0.2	2816	48.8	194

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